What is claimed is:

1. A data processing circuit for receiving as input a plurality of packet data including packet data of at least one channel from an application side, selecting packet data of a desired channel from the input plurality of packet data, and transmitting the selected packet data to a data transmission path, comprising:

a channel identification data extracting circuit for extracting channel identification data regarding a selected channel in said input packet data;

a comparison circuit for comparing said extracted channel identification data with channel specifying data regarding a predetermined selected channel;

a packet data validity instruction signal generation circuit for outputting a packet data validity instruction signal indicating whether said packet data is valid or not based on said comparison result; and

a transmission circuit for selecting said input packet data to said data transmission path when said packet data validity instruction signal is valid.

2. A data processing circuit as set forth in claim 1, wherein said channel identification data extraction circuit receives as input a packet data input timing signal for specifying an input timing of said

packet data from said application side and extracts channel identification data regarding a selected channel in said input packet data based on said packet data input timing signal.

3. A data processing circuit as set forth in claim 1, wherein said transmission circuit transmits insert data to said data transmission path at a timing indicating that said packet data validity instruction signal is invalid.

4. A data processing circuit as set forth in claim 3, wherein said insert data is information data regarding said selected channel.

5. A data processing circuit as set forth in claim 1, further comprising a memory circuit for storing said channel specifying data.

6. A data processing circuit as set forth in claim 5, further comprising a computer for writing said channel specifying data to said memory circuit.

7. A data processing circuit as set forth in claim 1, further comprising:

a transmission packet data memory circuit for storing packet data to be transmitted to said data transmission path;

wherein said transmission circuit selects said input packet data and writes it to a transmission

packet data memory circuit when said packet data validity instruction signal indicates validity.

8. A data processing circuit as set forth in claim 1, wherein said transmission circuit transmits said selected packet data to said data transmission path at predetermined intervals.

9. A data processing circuit as set forth in claim 1, wherein said data transmission path is a serial bus.